What is claimed is:

1. A method comprising:

selectively storing data in a memory array at different densities per cell; and

implementing error correction depending on the density of data storage.

2. The method of claim 1 including selectively storing data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

3. The method of claim 2 including using a higher density mode with double the number of threshold levels as a lower density mode.

4. The method of claim 3 including using a higher density mode with four threshold levels and a lower density mode using two threshold levels.

5. The method of claim 1 wherein implementing error correction code depending on the density of data storage includes determining whether data is in a higher or lower density mode and if the data is in a higher density mode, implementing error correction code and if the data is in a lower density mode, omitting error correction code.

6. The method of claim 5 including using a flag to indicate whether or not the data is in a lower or higher density mode.

7. The method of claim 5 including allowing overwriting when the data is stored in the lower density mode.

8. The method of claim 7 including preventing overwriting when the data is stored in the higher density mode.

9. The method of claim 1 including allowing overwriting of stored data when error correcting codes are not provided for that data.

10. The method of claim 1 including providing a multi-level memory cell array having a capacity of at least four levels.

11. The method of claim 10 including using at least two bits to represent said at least four levels.

12. The method of claim 11 including using one of said bits as a more significant bit and the other of said bits as a less significant bit.

13. The method of claim 12 wherein data from at least two cells forms a codeword and grouping the more significant bits from different cells together.

14. The method of claim 13 including providing more significant bits in one half of a word and less significant bits in the other half of a word.

15. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

selectively store data in a memory array at different densities per cell; and

implement error correction depending on the density of data storage.

16. The article of claim 15 further storing instructions that, if executed, enable the system to selectively store data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

17. The article of claim 16 further storing instructions that, if executed, enable the system to use a higher density mode with double the number of threshold levels as a lower density mode.

18. The article of claim 17 further storing instructions that, if executed, enable the system to use a higher density mode with four threshold levels and a lower density mode using two threshold levels.

19. The article of claim 15 further storing instructions that, if executed, enable the system to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implement error correction code and if the data is in a lower density mode, omit error correction code.

20. The article of claim 19 further storing instructions that, if executed, enable the system to use a flag to indicate whether or not the data is in a lower or higher density mode.

21. The article of claim 19 further storing instructions that, if executed, enable the system to allow overwriting when the data is stored in a higher density mode.

22. The article of claim 20 further storing instructions that, if executed, enable the system to prevent overwriting when data is stored in the higher density mode.

23. The article of claim 15 further storing instructions that, if executed, enable the system to allow overwriting of stored data when error correcting codes are not provided for that data.

24. The article of claim 15 further storing instructions that, if executed, enable the system to provide a multi-level memory cell array having a capacity of at least four levels.

25. The article of claim 24 further storing instructions that, if executed, enable the system to use at least two bits to represent said at least four levels.

26. The article of claim 25 further storing instructions that, if executed, enable the system to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

27. The article of claim 26 wherein data from at least two cells forms a codeword and further storing instructions that, if executed, enable the system to group the more significant bits from different cells together.

28. The article of claim 27 further storing instructions that, if executed, enable the system to

provide more significant bits in one half of a codeword and less significant bits in the other half of a codeword.

29. A memory comprising:

a memory array; and

a controller coupled to said memory array to selectively store data in the memory array at different densities per cell and to implement error correction depending on the density of data storage.

30. The memory of claim 29 wherein said memory array is a multi-level flash memory array.

31. The memory of claim 29 wherein said controller to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implement error correction and if the data is in a lower density mode, omit error correction.

32. The memory of claim 31 said controller to allow overwriting when the data is stored in the lower density mode.

33. The memory of claim 32 said controller to prevent overwriting when the data is stored in the higher density mode.

34. The memory of claim 29 said controller to allow overwriting of stored data when error correcting code is not provided for that data.

35. The memory of claim 29 said controller to use at least two bits to represent four threshold voltage levels.

36. The memory of claim 35 said controller to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

37. The memory of claim 36 said controller to group the more significant bits from different cells together.

38. A system comprising:

a processor;

a wireless interface;

a memory coupled to said processor; and

a controller coupled to said memory to selectively store data in said memory at different densities per cell and to implement error correction depending on a density of data storage.

39. The system of claim 38 wherein said memory is a multi-level flash memory.

40. The system of claim 38 wherein said controller to determine whether data is in higher or lower density mode and if the data is in a higher density mode, implement error correction and if the data is in a lower density mode, omit error correction.

41. The system of claim 40 said controller to allow overwriting when the data is stored in the lower density mode.

42. The system of claim 41 said controller to prevent overwriting when the data is stored in the higher density mode.

43. The system of claim 38 said controller to allow overwriting of stored when error correcting codes are not provided for that data.

44. The system of claim 38 said controller to use at least two bits to represent four threshold levels.

45. The system of claim 44 said controller to use one of said bits as a more significant bit and the other said bits as a less significant bit.

46. The system of claim 45 said controller to group the more significant bits from different cells together.

47. The system of claim 38 wherein said wireless interface includes an antenna.

48. The system of claim 47 wherein said wireless interface includes a dipole antenna.